# BIKANER TECHNICAL UNIVERSITY, BIKANER
# बीकानेर तकनीकी विश्वविद्यालय, बीकानेर

# COURSE SCHEME AND SYLLABUS

## M. TECH.
## VLSI DESIGN

**M. Tech.**
**VLSI Design**
**Teaching and Examination Scheme**
**1st Year –I Semester**

| SN | Category | Course Code | Course Title | Contact hrs/week L | T | P | Marks Exam Hrs | IA | ETE | Total | Cr |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **THEORY** | | | | | | | | | | | |
| 1 | PCC | 1ECMVL1-01 | MOS Device Physics | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| 2 | | 1ECMVL1-02 | Digital VLSI Circuit Design | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| 3 | | 1ECMVL1-03 | Analog VLSI Circuit Design | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| 4 | PEC-I | 1ECMVL2-04 | VLSI Technology | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| | | 1ECMVL2-05 | VLSI System Design | | | | | | | | |
| | | 1ECMVL2-06 | Semiconductor Microwave Devices and Applications | | | | | | | | |
| | | 1ECMVL2-07 | ---------- | | | | | | | | |
| 5 | PEC-II | 1ECMVL2-08 | Semiconductor Materials, Devices & Characterization | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| | | 1ECMVL2-09 | VLSI Testing & Testability | | | | | | | | |
| | | 1ECMVL2-10 | Advanced VLSI Interconnects | | | | | | | | |
| | | 1ECMVL2-11 | ---------- | | | | | | | | |
| 6 | OES | 1ECMVL3-12 | Human Values and Professional Ethics | 2 | - | - | 3 | 20 | 80 | **100** | **2** |
| | | | **Sub Total** | 17 | | | | | | **600** | **17** |
| **PRACTICAL & SESSIONAL** | | | | | | | | | | | |
| 7 | PCC | 1ECMVL1-13 | Simulation Lab - I | - | - | 2 | - | 60 | 40 | **100** | **2** |
| 8 | FW | 1ECMVL4-14 | Field Work | - | - | 2 | - | 60 | 40 | **100** | **2** |
| 9 | AC | 1ECMVL5-15 | Human Values Practice School | - | - | 2 | - | 30 | 20 | **-** | **-** |
| | | | **Sub- Total** | | | 6 | | | | **200** | **4** |
| | | | **TOTAL OF I SEMESTER** | 17 | | 6 | | | | **800** | **21** |

***L:*** *Lecture,* ***T:*** *Tutorial,* ***P:*** *Practical,* ***Cr:*** *Credits,* ***ETE:*** *End Term Exam,* ***IA:*** *Internal assessment.*

**PCC:** Program Core Courses, **PEC:** Program Elective Courses
Electives Courses (3-4Nos.) should be relevant to the chosen specialization/branch

**OES:** Other Emerging Subjects: (i) Human Values and Professional Ethics
(ii) Research Methodology
It is decided common for all branches.

**FW:** Field Work
Student is required to work in the organization/industry concerned with his/her course.

**AC:** Audit Course
It is mandatory to pass the audit course. However, credit shall not be awarded.

**M. Tech.**
**VLSI Design**
**Teaching and Examination Scheme**
**1st Year –II Semester**

| THEORY | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **SN** | **Category** | **Course** | | **Contact hrs/week** | | | **Marks** | | | | **Cr** |
| | | **Code** | **Title** | **L** | **T** | **P** | **Exam Hrs** | **IA** | **ETE** | **Total** | |
| 1 | PCC | 2ECMVL1-01 | VLSI Physical Design | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| 2 | | 2ECMVL1-02 | Mixed Signal Circuit Design | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| 3 | | 2ECMVL1-03 | Nano-scale Devices | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| 4 | PEC-I | 2ECMVL2-04 | VLSI Digital Signal Processing | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| | | 2ECMVL2-05 | Performance and Reliability of VLSI Circuits | | | | | | | | |
| | | 2ECMVL2-06 | MEMS & NEMS | | | | | | | | |
| | | 2ECMVL2-07 | ---------- | | | | | | | | |
| 5 | PEC-II | 2ECMVL2-08 | CAD for VLSI | 3 | - | - | 3 | 20 | 80 | **100** | **3** |
| | | 2ECMVL2-09 | Optoelectronic Materials and Devices | | | | | | | | |
| | | 2ECMVL2-10 | Organic Electronics | | | | | | | | |
| | | 2ECMVL2-11 | ---------- | | | | | | | | |
| 6 | OES | 2ECMVL3-12 | Research Methodology | 2 | - | - | 3 | 20 | 80 | **100** | **2** |
| | | | **Sub Total** | 17 | | | | | | **600** | **17** |

| PRACTICAL & SESSIONAL | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 7 | PCC | 2ECMVL1-13 | Simulation Lab - II | - | - | 2 | - | 60 | 40 | **100** | **2** |
| 8 | FW | 2ECMVL4-14 | Field Work | - | - | 2 | - | 60 | 40 | **100** | **2** |
| | | | **Sub- Total** | | | 4 | | | | **200** | **4** |
| | | | **TOTAL OF I SEMESTER** | 17 | | 4 | | | | **800** | **21** |

**M. Tech.**
**VLSI Design**
**Teaching and Examination Scheme**
**2nd Year – III Semester**

| PRACTICAL & SESSIONAL | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **SN** | **Category** | **Course** | | **Contact hrs/week** | | | **Marks** | | | | **Cr** |
| | | **Code** | **Title** | **L** | **T** | **P** | **Exam Hrs** | **IA** | **ETE** | **Total** | |
| 1 | PSD | 3ECMVL6-16 | Industrial/Field Project | - | - | 28 | - | 360 | 240 | **600** | **14** |
| 2 | PSD | 3ECMVL6-17 | Seminar | - | - | 4 | - | 60 | 40 | **100** | **2** |
| | | **TOTAL OF III SEMESTER** | | | | 32 | | | | **700** | **16** |

**PSD:** Industrial/Field Project, Seminar, Dissertation

**M. Tech.**
**VLSI Design**
**Teaching and Examination Scheme**
**2nd Year – IV Semester**

| PRACTICAL & SESSIONAL | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **SN** | **Category** | **Course** | | **Contact hrs/week** | | | **Marks** | | | | **Cr** |
| | | **Code** | **Title** | **L** | **T** | **P** | **Exam Hrs** | **IA** | **ETE** | **Total** | |
| 1 | PSD | 4ECMVL6-18 | Dissertation | - | - | 32 | - | 420 | 280 | **700** | **16** |
| | | **TOTAL OF IV SEMESTER** | | | | 32 | | | | **700** | **16** |

**M. Tech.**
**VLSI Design**
**Syllabus**

## 1ECMVL1-01: MOS DEVICE PHYSICS

**MOS Capacitor:** Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, Midgap, and Inversion, 1D Electrostatics of MOS, Depletion Approximation, Accurate Solution of Poisson's Equation, CV characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges, Midgap gate Electrode, Poly-Silicon contact, Electrostatics of non-uniform substrate doping, ultrathin gate-oxide and inversion layer quantization.

**Physics of MOSFET:** Drift-Diffusion Approach for IV, Gradual Channel Approximation, Sub-threshold current and slope, Body effect, Pao & Sah Model, Detail 2D effects in MOSFET, High field and doping dependent mobility models, High field effects and MOSFET reliability issues, Leakage mechanisms in thin gate oxide, High-K-Metal Gate MOSFET devices and technology issues, Intrinsic MOSFET capacitances and resistances.

**SOI MOSFET**: FDSOI and PDSOI, 1D Electrostatics of FDSOI MOS, threshold voltage definitions, Back gate coupling and body effect parameter, IV characteristics of FDSOI-FET,

**Short-Channel MOSFETs:** Short-Channel MOSFETs, Short-Channel Effect, Velocity Saturation and High-Field Transport, Channel Length Modulation

FDSOI-sub-threshold slope, Floating body effect, single transistor latch, SRAM device.

Source–Drain Series Resistance, MOSFET Degradation and Breakdown at High Fields, MOSFET Scaling

**Nanoscale Transistors:** Physical view of the Nanoscale MOSFETs, Natori's theory of the ballistic MOSFET, ballistic MOSFET in general, degenerate and non-degenerate conditions. Scattering theory of MOSFET; scattering model, transmission coefficient under low and high drain bias.

**Suggested Readings:**


1. S.M. Sze & Kwok K. Ng, Physics of Semiconductor Devices, Wiley, 2007
2. Yuan Taur & Tak H. Ning, Fundamentals of Modern VLSI Devices, Cambridge, 2013
3. Mark Lundstrom& Jing Guo, Nanoscale Transistors: Device Physics, Modeling & Simulation, Springer, 2005
4. YannisTsividis, Operation and Modeling of the MOS Transistor, Oxford University Press, 2003
5. J.P. Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Springer, 1997

## 1ECMVL1-02: DIGITAL VLSI CIRCUIT DESIGN

Review of MOSFET operation and CMOS process flow: MOS Threshold voltage, MOSFET I-V characteristics: Long and short channel, MOSFET capacitances, lumped and distributed RC model for interconnects, transmission lines, CMOS process flow, Layout and design rules.

CMOS inverter: Static characteristics, power consumption, dynamic behavior, buffer design using the method of logical effort.

Combinational logic: Transistor sizing in static CMOS logic gates, static CMOS logic gate sizing considering method of logical effort, dynamic logic, pass-transistor logic, common mode and other cross-coupled logic families.

Sequential logic: Static latches and flip-flops (FFs), dynamic latches and FFs, sense-amplifier based FFs, NORA-CMOS, Schmitt trigger, monostable and astable circuits.

Memories and array structures: MOS-ROM, SRAM cell, memory peripheral circuits, signal to noise ratio, power dissipation, timing issues.

**Suggested Readings:**


1. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective," Prentics Hall, 2003
2. Sung-Mo Kang, Yusuf Liblebici, "CMOS Digital Integrated Circuits," Tata Mc Graw Hill, 2003.
3. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design," Wiley India Pvt. Ltd. 2009
4. Ivan Sutherland, R. Sproull and D. Harris, "Logical Effort: Designing Fast CMOS Circuits", Morgan Kaufmann, 1999.


## 1ECMVL1-03: ANALOG VLSI CIRCUIT DESIGN

**CMOS Device Fundamentals**: Motivation for analog VLSI and mixed signal circuits in CMOS technologies and issues thereof, Basic MOS models, device capacitances, parasitic resistances, substrate models, transconductance, output resistance, unity gain bandwidth, frequency dependence of device parameters.

**Current Mirrors, Current and Voltage Reference:** Basic current mirrors, cascode current mirrors, active current mirrors, low current biasing, supply insensitive biasing, temperature insensitive biasing, impact of device mismatch.

**Single Stage and Differential Amplifiers:** Common source amplifier, source degeneration, source follower, common gate amplifier, cascade stage, Basic differential pair, common mode response, differential pair with MOS loads, Gilbert Cell, device mismatch effects, input offset voltage.

**Frequency Response of Amplifiers:** Miller effect, CS amplifier, source follower, CG amplifier, cascade stage, differential amplifier, Multistage amplifier, feedback topology and their impact on amplifier design, types of Noise and their statistical characteristics.

**Operational Amplifiers:** Performance parameters, One-stage and two-stage Op Amps, gain boosting, comparison, common mode feedback, input range, slew rate, power supply rejection, noise in Op Amps, Stability and Frequency Compensation.

**Suggested Readings:**


1. Razavi, B., "Design of Analog CMOS Integrated Circuits", 1st Ed., McGraw Hill., 2016
2. Gray, P.R., Hurst, P. J., Lewis, S.H., Meyer, R.G., "Analysis and Design of Analog Integrated Circuits", 4th Ed., John Wiley and Sons., 2009
3. Baker, R. J., Li, H. W. and Boyce, D. E., "CMOS Circuit Design
4. ,Layout and Simulation", Prentice-Hall of India., 1999.


## 1ECMVL2-04: VLSI TECHNOLOGY

**Introduction to VLSI Technology:** Device scaling and Moore's law, basic device fabrication methods, alloy junction and planar process, Czochralski and Bridgman techniques, Characterization methods and wafer specifications, defects in Si and GaAs.

**Oxidation:** Surface passivation using oxidation. Deal-Grove model, oxide characterization, types of oxidation and their kinematics, thin oxide growth models, stacking faults, oxidation systems.

**Diffusion and Ion-Implantation:** Solutions of diffusion equation, diffusion systems, ion implantation technology, ion implant distributions, implantation damage and annealing, transient enhanced diffusion and rapid thermal processing.

**Epitaxy and Thin Film Deposition:** Thermodynamics of vapor phase growth, MOCVD, MBE, CVD, reaction rate and mass transport limited depositions, APCVD/LPVD, equipments and applications of CVD, PECVD, and PVD.

**Etching and Lithography:** Wet etching, selectivity, isotropy and etch bias, common wet etchants, orientation dependent etching effects; Introduction to plasma technology. Optical lithography contact/proximity and projection printing, resolution and depth of focus, resist processing methods and resolution enhancement, X-ray lithography.

**Suggested Readings:**


1. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall., 2000
2. Sze, S.M., "VLSI Technology", 4th Ed., Tata McGraw Hill., 1999
3. Chang, C.Y. and Sze, S.M., "ULSI Technology", McGraw-Hill., 1996

4. Gandhi, S. K., "VLSI Fabrication Principles: Silicon and Gallium Arsenide", John Wiley and Sons, 2003
5. Campbell, S.A., "The Science and Engineering of Microelectronic Fabrication", 4th Ed., Oxford University Press., 1996.

## 1ECMVL2-05: VLSI SYSTEM DESIGN

Introduction to Placement and Routing, PNR and Routing, Placement Optimisation, Routing Algorithms and its application to simple design issues.

behavior analysis using state diagrams, STA using clock jitters, Example Study for a real chip, Multiple Clock, data transition with respect to power analysis, Clock Tree synthesis- H-tree, Buffering, Synthesis timing, set-up analysis with multiple clock.

Introduction to Static Timing Analysis, STA with ideal clocks, flip-flop

Stack subsystem design, control timing, generation of control singnals. Register to Register Transfer. Combinational Logic. The Programmable Logic Array. Basic concept, Circuit design, and stick diagram of example. Finite State Machines.

Datapath Operators, Adder, Parity Generator, Comparator ALU, Multiplexer Multiplier, Shifter.

Layout Generation: Partitioning, Floor Planning, Placement, Routing–Global, Channel and Switch box Routing, Power and Clock distribution, Pad Design.

**Suggested Readings:**

1. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic 'Digital Integrated Circuits: A Design Prespective. Second Edition, A Prentice-Hall Publication Hall, 2003
2. N.Weste and D.Harris, "CMOS VLSI Design: Circuits and Systems Perspective," Fourth edition, Addison Wesley., 2010

## 1ECMVL2-06: SEMICONDUCTOR MICROWAVE DEVICES AND APPLICATIONS

Transient and ac behaviour of p-n junctions, effect of doping profile on the capacitance of p-n junctions, noise in p-n junctions, high-frequency equivalent circuit, varactor diode and its applications; Schottky effect, Schottky barrier diode and its applications; Heterojunctions.

Tunneling process in p-n junction and MIS tunnel diodes, V-I characteristics and device performance, backward diode. Impact ionization, IMPATT and other related diodes, small signal analysis of IMPATT diodes.

Two-valley model of compound semiconductors, Vd-E characteristics, Gunn effect, modes of operation, small-signal analysis of Gunn diode, power frequency limit, Construction and operation of microwave PIN diodes, equivalent circuit, PIN diode switches, limiters and modulators.

High frequency limitations of BJT, microwave bipolar transistors, heterojunction bipolar transistors; Operating characteristics of MISFETs and MESFETs, short-channel effects, high electron mobility transistor.

Characteristics and design of microstrips, slotlines and coplanar Waveguides, Design considerations for microwave and millimeter wave amplifiers and oscillators, circuit realization, noise performance.

**Suggested Readings:**


1. Sarrafzadeh, M. and Wong, C.K., "An Introduction to VLSI Physical Design", 4th Ed., McGraw-Hill., 1996
2. Wolf, W., "Modern VLSI Design System on Silicon", 2nd Ed., Pearson Education., 2000
3. Sait, S.M. and Youssef, H "VLSI Physical Design Automation: Theory and practice", World scientific., 1999
4. Dreschler, R., "Evolutionary Algorithm for VLSI CAD", 3rd Ed., Springer, 2002
5. Sherwani, N.A., "Algorithm for VLSI Physical Design Automation", 2nd ED., Kluwer., 1999
6. Lim, S.K., "Practical problems in VLSI physical Design Automation", Springer., 2008


## 1ECMVL2-08: SEMICONDUCTOR MATERIALS, DEVICES & CHARACTERIZATION

**Semiconductor Physics:** Band structure, carrier energy and Fermi distributions for free carriers, donor and acceptor impurities, determination of band gap, impurity ionization, and critical temperatures for intrinsic ionization and onset of impurity deionization, excess carriers and current transport.

**Junction Diode:** p-n junction, tunnel diode, quasi Fermi levels, depletion width capacitance and its application in doping profile determination, I-V characteristics of narrow and wide base diodes and their equivalent circuits, breakdown mechanisms, small signal ac impedance.

**Bipolar Transistor Fundamentals:** Formation of transistor, n–p–n Transistors, Ideal Current–Voltage Characteristics, Characteristics of a Typical n–p–n Transistor, Bipolar Device Models for Circuit and Time-Dependent Analyses, Breakdown Voltages.

**Surface Field Effect Transistors**: Surface states, measurement of surface charge, Q-V/I-V characteristics and equivalent circuit models of MOS capacitor and MOSFET.

**Metal-Semiconductor Junctions**: Rectifying and ohmic contacts, role of surface states, application in energy level characterization; Comparison of p-n junction and Schottky diodes.

**Suggested Readings:**


1. Rabaey, J.M., Chandrakasan, A. and Nikolic B., "Digital Integrated Circuits: A Design Perspective", 2nd Ed., PrenticeHall of India., 2006
2. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits: Analysis and Design", Tata McGraw-Hil., 2003
3. Ben G. Streetman & Sanjay Banerjee, "Solid State Electronic devices" PHI., 2009
4. Eshraghian, K., Pucknell, D.A. and Eshraghian, S., "Essentials of VLSI Circuit and System", 2nd Ed., Prentice-Hall of India., 2005.


## 1ECMVL2-09: VLSI TESTING & TEST ABILITY

Motivation for testing, Design for testability, the problems of digital and analog testing, Design for test, Software testing. Faults in Digital Circuits: Controllability, and Observability, Fault models - stuck-at faults, Bridging faults, intermittent faults.

Digital Test Pattern Generation: Test pattern generation for combinational logic circuits, Manual test pattern generation, Automatic test pattern generation - Roth's D-algorithm, Developments following Roth's D algorithm, Pseudorandom test pattern generation, Test pattern generation for sequential circuits, Exhaustive, non-exhaustive and pseudorandom 70 test pattern Generation, Delay fault testing.

Signatures and Self Test: Input compression output compression arithmetic, Reed- Muller and spectral coefficients, Arithmetic and Reed-Muller coefficients, Spectral coefficients, Coefficient test signatures, Signature analysis and online self test.

Testing of Analog and Digital circuits: Testing techniques for Filters, A/D Converters, Programmable logic devices and DSP, Test generation algorithms for combinational logic circuits – fault table, Boolean difference, Path sensitilization, D-algorithm, Fault simulation techniques, Built–in-Self test, PLA test and DFT.

Memory Design and Testing: Memory Fault Modeling, testing, And Memory Design For Testability And Fault Tolerance RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing.

**Suggested Readings:**


1. M. L. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory,and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers., 2000
2. A.K Sharma, Semiconductor Memories Technology, Testing and Reliability, IEEE Press.

## 1ECMVL2-10: ADVANCED VLSI INTERCONNECTS

**Preliminary Concepts**

Interconnects for VLSI applications, metallic interconnects, optical interconnects, superconducting interconnects, advantages of copper interconnects, challenges posed by copper interconnects, fabrication process, even and odd mode capacitances, transmission line equations, resistive interconnection as ladder network.

**Parasitic Extraction**

Parasitic resistance, effect of surface/interface scattering and diffusion barrier on resistance, Capacitance: parallel-plate capacitance, fringing capacitance, coupling capacitance, methods of capacitance extraction, Inductance: self inductance, mutual inductance, methods of inductance extraction, high frequency losses, skin effect, dispersion effect.

**Modeling of Interconnects and Crosstalk Analysis**

Elmore model, Transfer function model, even and odd mode model, Time domain analysis of multiconductor lines, Finite Difference Time Domain (FDTD) method, performance analysis using linear resistive driver and nonlinear CMOS driver, advanced interconnect techniques to avoid crosstalk.

**Future VLSI Interconnects**

Optical interconnects, Superconducting interconnects, Nanotechnology interconnects, Silicon nanowires, Carbon nanotubes, Graphene nanoribbons: system issues and challenges, material processing issues and challenges, design issues and challenges.

**Carbon Nanotube and Graphene Nanoribbon VLSI Interconnects**

Quantum electrical properties: quantum conductance, quantum capacitance, kinetic inductance, Carbon nanotube (CNT) and Graphene nanoribbon (GNR)
interconnects, electron scattering and lattice vibrations, electron mean free path, single-wall CNT and single layer GNR resistance model, performance comparison of CNTs, GNRs and copper interconnects.

**Suggested Readings:**


1. High-Speed VLSI Interconnects, Ashok K. Goel, 1987
2. Advanced Nanoscale ULSI Interconnects: Fundamentals and Applications, Y.S. Diamand, 2007
3. Carbon nanotube and Graphene Device Physics, H.S Philip Wong and Deji Akinwande, 2009

## 1ECMVL3-12: HUMAN VALUES AND PROFESSIONAL ETHICS

**Need, Basic Guidelines, Content And Process For Value Education:**
Understanding the need, basic guidelines, Self Exploration - its content and process; 'Natural Acceptance' and Experiential Validation, Continuous Happiness and Prosperity- Human Aspirations, Right understanding, Relationship and Physical Facilities, Understanding Happiness and Prosperity correctly- A critical appraisal of the current scenario. Method to fulfill the above human aspirations: understanding and living in harmony at various levels

**Understanding Harmony in the Human Being - Harmony in Myself:**
Understanding human being as a co-existence of the sentient 'I' and the material 'Body' Understanding the needs of Self ('I') and 'Body' - Sukh and Suvidha Understanding the Body as an instrument of 'I', Understanding the characteristics and activities of 'I' and harmony in 'I' Understanding the harmony of I with the Body: Sanyam and Swasthya; correct appraisal of Physical needs, meaning of Prosperity in detail, Programs to ensure Sanyam and Swasthya.

**Understanding Harmony in the Family and Society- Harmony in Human-Human Relationship:**
Understanding harmony in the Family, Understanding values in human-human relationship; meaning of Nyaya and program for its fulfillment to ensure Ubhay-tripti; Trust (Vishwas) and Respect (Samman) , meaning of Vishwas; Difference between intention and competence, meaning of Samman, Difference between respect and differentiation; the other salient values in relationship, harmony in the society , Samadhan, Samridhi, Abhay, Sah-astitva as comprehensive Human Goals ,Visualizing a universal harmonious order in society- Undivided Society (AkhandSamaj), Universal Order (SarvabhaumVyawastha )- from family to world family.

**Understanding Harmony in the Nature and Existence - Whole Existence as Coexistence:**
Understanding the harmony in the Nature. Interconnectedness and mutual fulfillment among the four orders of nature- recyclability and self-regulation in nature. Understanding Existence as Co-existence (Sah-astitva) of mutually interacting units in all pervasive Space. Holistic perception of harmony at all levels of existence

**Implications of the Above Holistic Understanding of Harmony on Professional Ethics - Natural Acceptance of Human Values:**
Definitiveness of Ethical Human Conduct. Basis for Humanistic Education, Humanistic Constitution and Humanistic Universal Order. Competence in Professional Ethics: a) Ability to utilize the professional competence for augmenting universal human order, b) Ability to identify the scope and characteristics of people-friendly and eco-friendly production systems, technologies and management models. Strategy for transition from the present state to Universal Human Order: At the level of individual: as socially and ecologically responsible engineers, technologists and managers. Case studies related to values in professional life and individual life.

**Suggested Readings:**


1. R. R. Gaur, R Sangal, G P Bagaria, A Foundation Course in Human Values and Professional Ethics, Excel Books, 2009. ISBN: 978-9-350-62091-5
2. R. Subramanian, Professional Ethics includes Human Values, Oxford Univ. Press.
3. A. N. Tripathy, 2003, Human Values, New Age International Publishers.
4. M Govindrajran, S Natrajan & V.S. Senthil Kumar, Engineering Ethics (including Human Values), Eastern Economy Edition, Prentice Hall of India Ltd.
5. B P Banerjee, 2005, Foundations of Ethics and Management, Excel Books.
6. B L Bajpai, 2004, Indian Ethos and Modern Management, New Royal Book Co., Lucknow. Reprinted 2008.


## 1ECMVL1-13: SIMULATION LAB – I

Design, implement and experiment with digital system, this will include ASIC design, FPGA based design. design of relevant hardware and software for microcontroller, processor and DSP based embedded system.

Custom design and simulation of different higher level analog and digital circuits using advance EDA tools like Tanner Spice S-edit and L- edit.

## 1ECMVL4-14: FIELD WORK

Student is required to work in the organization/industry concerned with his/her course.

## 1ECMVL5-15: HUMAN VALUES PRACTICE SCHOOL

This practice school in first semester will have two parts -

### I. Industry Interaction

In this, students will start his industry interaction in the very first semester of the M.Tech. Course. He/ She has to visit an organization for 3 hours /week in any industry finalized/selected by competent authority. This interaction will give him feel and insight to the real time working.

A. This 3 hours /work will be after the classroom studies
B. Selection criteria of organisation-
   1. Have turnover more than 20 lakhs
   2. Have more than 20 employees

C. During these hours, student will observe following points in the organisation:
   1. Organisational structure and hierarchy
   2. Different kind of jobs/works done by the employees at all levels in the company

3. Working of different departments
4. Types of skills require to work in an organisation
5. Ways of internal and external communication
6. Formal dressing and attitude
7. Coordination and team work

**II. Social Responsibility**

To make students understand his role and responsibility in society & nature and co-existence as whole, student has to take an initiative towards contribution in any relevant social and environmental issue.

A. This work will be performed after the time of regular classes

B. Student will perform one or more of the following activities after the approval of mentor and HOD:

1. Making contribution in increasing the income of any street vender or any needy person from under privileged section
2. Cleanliness Campaign
3. Donation of his/her belongings which is of no use to him/her to needy ones
4. Plantation and care for nature (soil, natural resources, plants and animals)
5. Girl child and women safety, education and empowerment.
6. Blood donations and help of needy people at hospitals
7. Helping the under – privileged section of the society
8. Educating the street children or in schools when and where needed.
9. Nukkad Natak on any topic of social or environmental concern.
10. Any other relevant activities.

## 2ECMVL1-01: VLSI PHYSICAL DESIGN

**Introduction:** Layout and design rules, materials for VLSI fabrication, basic algorithmic concepts for physical design, physical design processes and complexities.

**Partition:** Kernigham-Lin's algorithm, Fiduccia Mattheyes algorithm, Krishnamurty extension, hMETIS algorithm, multilevel partition techniques.

**Floor-Planning:** Hierarchical design, wirelength estimation, slicing and non-slicing floorplan, polar graph representation, operator concept, Stockmeyer algorithm for floor planning, mixed integer linear program.

**Placement:** Design types: ASICs, SoC, microprocessor RLM; Placement techniques: Simulated annealing, partition-based, analytical, and Hall's quadratic; Timing and congestion considerations.

**Routing:** Detailed, global and specialized routing, channel ordering, channel routing problems and constraint graphs, routing algorithms, Yoshimura and Kuh's method, zone scanning and net merging, boundary terminal problem, minimum density spanning forest problem, topological routing, cluster graph representation.

**Suggested Readings:**


1. Sarrafzadeh, M. and Wong, C.K., "An Introduction to VLSI Physical Design", 4th Ed., McGraw-Hill., 1996
2. Wolf, W., "Modern VLSI Design System on Silicon", 2nd Ed., Pearson Education., 2000
3. Sait, S.M. and Youssef, H., "VLSI Physical Design Automation: Theory and Practice", World Scientific., 1999
4. Dreschler, R., "Evolutionary Algorithms for VLSI CAD", 3rd Ed., Springer, 2002
5. Sherwani, N.A., "Algorithm for VLSI Physical Design Automation", 2nd Ed., Kluwer, 1999
6. Lim, S.K., "Practical Problems in VLSI Physical Design Automation", Springer., 2008


## 2ECMVL1-02 MIXED SIGNAL CIRCUIT DESIGN

**Sampling and Aliasing:** Impulse Sampling, Decimation, K-Path Sampling Sample-and-Hold, Track-and-Hold, Implementation of S/H, Discrete Analog Integrator.

**Analog Filters:** Integrator building blocks, MOSFET-C Integrator $g_m$-CIntegrators, Discrete time Integrators, Filtering topologies, Bilinear and Biquadratic Transfer function

**Digital Filters:** SPICE Models for DACs and ADCs, Sinc Shaped digital filters, Bandpass and Highpass sinc Filters, Filtering topologies, FIR Filter, Concept of stability and Overflow.

**Digital Filters:** SPICE Models for DACs and ADCs, Sinc Shaped digital filters, Bandpass and Highpass sinc Filters, Filtering topologies, FIR Filter, Concept of stability and Overflow,

**Data Convertor Design:** One bit ADC and DAC, Passive Noise shaping, Improving SNR and Linearity, Improving Linearity using Active circuits, First Order Noise Shaping, Second order noise shaping, noise shaping topologies, Cascaded Modulators.

**Suggested Readings:**


1. Baker Jacob R, "CMOS Mixed signal Circuit Design," Wiley IEEE Press., 2010
2. Razavi, B., "Design of Analog CMOS Integrated Circuits", 1st Ed., McGraw Hill., 2001
3. David Johns, Ken Martin, "Analog Integrated Circuit Design",John Wiley and Sons., 1997
4. Behzad Razavi, "Principles of Data Conversion System Design", *Wiley-IEEE Press*., 1994
5. Rudy van de Plassche, "Integrated Analog-to-Digital and Digital-to-Analog Converters", *Springer*., 2003.

## 2ECMVL1-03: NANO-SCALE DEVICES

**CMOS scaling challenges in nanoscale regimes:** Moor and Koomey's law, Leakage current mechanisms in nanoscale CMOS, leakage control and reduction techniques, process variations in devices and interconnects.

**Device and technologies for sub 100nm CMOS:** Silicidation and Cu-low k interconnects, strain silicon – biaxial stain and process induced strain; Metal-high k gate; Emerging CMOS technologies at 32nm scale and beyond – FINFETs, surround gate nanowire MOSFETs, heterostructure (III-V) and Si-Ge MOSFETs.

**Device scaling and ballistic MOSFET:** Two dimensional scaling theory of single and multigate MOSFETs, generalized scale length, quantum confinement and tunneling in MOSFTEs, velocity saturation, carrier back scattering and injection velocity effects, scattering theory of MOSFETs.

**Emerging nanoscale devices:** Si and hetero-structure nanowire MOSFETs, carbon nanotube MOSFETs, Tunnel FET, quantum wells, quantum wires and quantum dots; Single electron transistors, resonant tunneling devices.

**Non-classical CMOS:** CMOS circuit design using non-classical devices – FINFETs, nanowire, carbon nanotubes and tunnel devices.

**Suggested Readings:**


1. Lundstrom, M., "Nanoscale Transport: Device Physics, Modeling, and Simulation", Springer., 2005
2. Maiti, C.K., Chattopadhyay, S. and Bera, L.K., "Strained-Si and Hetrostructure Field Effect Devices", Taylor and Francis., 2007
3. Hanson, G.W., "Fundamentals of Nanoelectronics", Pearson India., 2008
4. Wong, B.P., Mittal, A., Cao Y. and Starr, G., "Nano-CMOS Circuit and Physical Design", Wiley., 2004
5. Sandip Kundu, Aswin Sreedhar, "Nanoscale CMOS VLSI Circuits: Design for Manufacturability" McGraw Hill 2010


## 2ECMVL2-04: VLSI DIGITAL SIGNAL PROCESSING

**Introduction to DSP Systems**: Typical DSP programs, Area-speed-power tradeoffs, Representation methods of DSP systems, Iteration, Iteration period, Iteration bound, Algorithms to compute iteration bound – Longest path matrix, Minimum cycle matrix.

**Pipelining and Parallel Processing**: Introduction to pipelining and parallel processing, Pipelining of FIR digital filters, Parallel processing, Pipelining and parallel processing for low power

**Unfolding Folding:** Retiming concept**,** Algorithm for unfolding, Properties of unfolding, Application of unfolding, Sample period reduction, Word and bit-level parallel processing, Folding technique, Folding transformation, Retiming for folding.

**Fast Convolution:** Introduction, Cook-Toom algorithm and modified Cook Toom algorithm, Winograd algorithm and modified Winograd algorithm, Iterated convolution, Cyclic onvolution, Design of Fast convolution algorithm by inspection

FIR and IIR Filters: Introduction, Parallel FIR filters, Two-parallel and three-parallel low-complexity FIR filters, Discrete Cosine Transform and Inverse DCT, Pipeling in 1st and 2nd order IIR digital filters, Pipelining in higher order IIR digital filters.

**Suggested Readings:**


1. Parhi, Keshab K., "VLSI Digital Signal Processing Systems: Design and Implementation", John Willey & Sons., 1999
2. John G. Proakis, Dimitris Manolakis: Digital Signal Processing: Principles, Algorithms and Applications, 4th ed, Pearson., 2006
3. Sen M. Kuo, Woon-Seng Gan: Digital Signal Processors: Architectures, Implementations, and Applications, Prentice Hall., 2005


## 2ECMVL2-05: PERFORMANCE AND RELIABILITY OF VLSI CIRCUITS

**Nanoscale MOSFET Characteristics:** Quasi-ballistic I-V characteristics, terminal capacitances of transistors considering quantum effects, parasitic resistances in nanoscale MOSFETs.

**Delay and Timing Models:** Classical delay models of logic gates, logic gate delay models for nano-regime CMOS technologies, timing parameters of sequential circuit elements, access-time of CMOS memories, impact of process/temperature/supply-voltage variations on timing parameters.

**Power Consumption:** Models for dynamic power, short circuit power and leakage power of CMOS circuits, full-chip power estimation techniques, impact of process/temperature variations on power consumption.

**Reliability of CMOS Circuits:** Circuit performance considering NBTI/PBTI, oxide breakdown, random telegraph noise, radiation damage.

**Analog Circuit Performance Parameters:** Impact of parasitic effects, process/temperature variation, device reliability effects.

**Suggested Readings:**


1. Yuan Taur and T. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press., 1998
2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, "Digital Integrated Circuits: A Design Perspective," Prentics Hall, 2003

3. Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, Tata McGraw-Hill., 2002

## 2ECMVL2-06: MEMS & NEMS

**Introduction to Micro-fabrication:** Cleaning, Oxidation, Diffusion, Mask making, Lithography, Etching, Ion Implantation, CVD, PVD, Metallization; Surface micromachining and Bulk Micromachining, DRIE, LIGA, Fabrication of high aspect ratio deformable structures.

**Elasticity in Materials:** Stress, strain calculations, Normal and Shear strains and constitutive relations, Plane stress, biaxial stress, residual stress, energy relations, Load-deflection calculations in beams, cantilevers (rectangular cross section), Elastic deformation in square plate, Resonant frequency calculations: Rayleigh-Ritz method.

MEMS Capacitive Switch: Lumped model, pull-in voltage, Electromechanical deflection modeling, pull-in instability, switching time and pull-in voltage scaling, Physical effects in nanoscale gap-size, squeeze-film damping perforated MEMS Capacitive switch, Comb actuators, Accelerometer, Pressure sensor, Energy approach: Lagrangian Mechanics applicable to MEMS capacitive switches, Reliability in RF-capacitive switch.

MEMS Sensors: Thermal sensor, Interaction of Thermal-Electrical Fields, Numerical design of thermal sensors, Bio-MEMS design problems.

Optical MEMS:2-D, 3-D switches, design examples.

**Suggested Readings:**

1. Lin, S. and Costello Jr., D.J., “Error Control Coding”, 2nd Ed., Pearson Prentice-Hall., 2004
2. Blahut, R.E., “Algebraic Codes for Data Transmission”, 2nd Ed., Cambridge University Press., 2003
3. Vucetic, B. and Yuan, J., “Turbo Codes: Principles and Applications”, Springer., 2000
4. McEliece, R., “Theory of Information and Coding”, 2nd Ed., Cambridge University Press., 2002
5. Huffman, W.C. and Pless, V., “Fundamentals of Error Correcting Codes”, Cambridge University Press., 2003
6. Moon, T.K., “Error Correction Coding: Mathematical Methods and Algorithms”, Wiley Interscience., 2005

## 2ECMVL2-08: CAD for VLSI

Evolution of design automation; CMOS realizations of basic gates, Behavioral, structural and physical models, design flow.

Types of CAD tools, introduction to logic simulation and synthesis, Syntax, hierarchical modeling, Verilog/VHDL construct, simulator directives, instantiating modules, gate level modeling

Delay modeling: Event based and level sensitive timing control, memory initialization, conditional compilation, time scales for simulation, Static timing analysis, delay, switch level modeling, user defined primitive (UDP), memory modeling.

Logic synthesis of HDL construct, technology cell library, design constraints, synthesis of Verilog/VHDL construct.

FPGAs based system design: Commercial FPGA architecture, LUT and routing architecture, FPGA CAD flow; Typical case studies.

**Suggested Readings:**


1. Weste, N. and Eshraghian, K., "Principles of CMOS VLSI Design –A Systems Perspective", 2nd Ed., Addison Wesley., 2006
2. Palnitkar, S., "Verilog HDL", 2nd Ed., Pearson Education. 2004
3. Wolf, W., "Modern VLSI Design: System on Chip", 2nd Ed., Prentice Hall of India., 2002


## 2ECMVL2-09: OPTOELECTRONIC MATERIALS AND DEVICES

Optical processes in semiconductors, EHP formation and recombination, absorption and radiation in semiconductor, deep level transitions, Auger recombination, luminescence and time resolved photoluminescence, optical properties of photonic band-gap materials.

Junction photodiode: PIN, heterojunction and avalanche photodiode; Comparisons of various photodetectors, measurement techniques for output pulse.

Photovoltaic effect, V-I characteristics and spectral response of solar cells, heterojunction and cascaded solar cells, Schottky barrier and thin film solar cells, design of solar cell.

Modulated barrier, MS and MSM photodiodes; Wavelength selective detection, coherent detection; Microcavity photodiode. Dynamic effects of MOS capacitor, basic structure and frequency response of charge coupled devices, buried channel charge coupled devices.

Electroluminescent process, choice of light emitting diode (LED) material, device configuration and efficiency; LED: Principle of operation, LED structure, frequency response, defects, and reliability and laser diode.

**Suggested Readings:**


1. Liao, S.Y., "Microwave Devices and Circuits", 4thEd., Pearson Education., 2002
2. Rebeiz, M.G., "R.F. MEMS: Theory, Design and Technology", 2nd Ed., Wiley-Interscience., 2003
3. Sze, S.M., and Ng, K.K., "Physics of Semiconductor Devices", 3rdEd. Wiley-Interscience., 2006
4. Glover, I.A., Pennoek, S.R. and Shepherd P.R., "Microwave Devices, Circuits and Sub-Systems", 4th Ed., John Wiley & Sons., 2005

## 2ECMVL2-10: ORGANIC ELECTRONICS

**Organic and Inorganic Materials & Charge Transport:** Introduction; Organic Materials: Conducting Polymers and Small Molecules, Organic Semiconductors: p-type, n-type, Ambipolar Semiconductors, Charge Transport in Organic Semiconductors, Charge Transport Models, Energy Band Diagram, Organic and inorganic materials for: Source, Drain and Gate electrodes, Insulators, Substrates; Comparison between Organic and Inorganic Semiconductors.

**Device Physics and Structures:** Organic Thin Film Transistors: Overview of Organic Field Effect Transistor (OFET); Operating Principle; Classification of Various Structures of OFETs; Output and Transfer Characteristics; OFETs Performance Parameters: Impact of Structural Parameters on OFET; Extraction of Various Performance Parameters, Advantages, Disadvantages & Limitations.

**Organic Device Modeling and Fabrication Techniques:** Modeling of OTFT Different Structures, Origin of Contact Resistance, Contact Resistance Extraction, Analysis of OFET Electrical Characteristics, Validation and Comparison of OFETs. Organic Devices and Circuits Fabrication Techniques.

**OLEDs and Organic Solar Cells Organic Light Emitting Diodes (OLEDs):** Introduction; Different Organic Materials for OLEDs; Classification of OLEDs, Output and Transfer Characteristics; Various Optical, Electrical and Thermal properties, Advantages, Disadvantages and Limitations. Organic Solar Cells: Introduction, Materials, various properties, Characteristics, Advantages, Disadvantages and Limitations and Applications.

**OTFT Applications Organic Inverters:** Inverter Circuits based on Different Materials Combination and Configurations; All-p-type, Organic Complementary Inverter Circuits, Hybrid Complementary Inverters, Comparison between All P-Type, Fully Organic and Hybrid Complementary Inverter Circuits; Logic Circuit Implementation; Organic Memory: Organic Static Random Access Memory (OSRAM) Organic DRAM, Shift registers and other Important Organic Memory Designs. OTFT as Driver for organic Light Emitting Diodes (OLEDs). Addition of More Applications based on Recent Technology Development.

**Suggested Readings:**


1. Hagen Klauk, Organic Electronics: Materials, Manufacturing and Applications, Wiley-VCH Verlag Gmbh & Co. KGaA, Germany., 2006
2. Klaus Mullen, Ullrich Scherf, Organic Light Emitting Devices: Synthesis, Properties and Applications, Wiley-VCH Verlag Gmbh & Co. KGaA, Germany., 2005
3. Dresselhaus, M.S., Dresselhaus, G. and Avouris, P., Carbon Nanotubes: Synthesis, Structure, Properties and Applications. New York: Springer- Verlag, 2001
4. Wolfgang Brutting, Physics of Organic Semiconductors, Wiley VCH Verlag Gmbh & Co. KGaA, Germany., 2005
5. Flora Li, Arokia Nathan, Yiliang Wu, Beng S. Ong, Organic Thin Film Transistor Integration: A Hybrid Approach, Wiley-VCH, Germany; 1st Ed., 2011

## 2ECMVL3-12: RESEARCH METHODOLOGY

**Research Methodology**: Objectives and Motivation of Research, Types of Research, Research Approaches, Significance of Research, Research Methods verses Methodology, Research and Scientific Method, Important of Research Methodology, Research Process, Criteria of Good Research, Problems Encountered by Researchers in India, Benefits to the society in general. Defining the Research Problem: Definition of Research Problem, Problem Formulation, Necessity of Defining the Problem, Technique involved in Defining a Problem.

**Literature Survey:** Importance of Literature Survey, Sources of Information, Assessment of Quality of Journals and Articles, Information through Internet. Literature Review: Need of Review, Guidelines for Review, Record of Research Review.

**Research Design:** Meaning of Research Design, Need of Research Design, Feature of a Good Design Important Concepts Related to Research Design, Different Research Designs, Basic Principles of Experimental Design, Developing a Research Plan, Design of Experimental Set-up, Use of Standards and Codes.

**Data Collection:** Collection of primary data, Secondary data, Data organization, Methods of data grouping, Diagrammatic representation of data, Graphic representation of data. Sample Design, Need for sampling, some important sampling definitions, Estimation of population, Role of Statistics for Data Analysis, Parametric V/s Non Parametric methods, Descriptive Statistics, Measures of central tendency and Dispersion, Hypothesis testing, Use of Statistical software. Data Analysis: Deterministic and random data, Uncertainty analysis, Tests for significance: Chisquare, student's t-test, Regression modeling, Direct and Interaction effects, ANOVA, F-test, Time Series analysis, Autocorrelation and Autoregressive modeling.

**Research Report Writing:** Format of the Research report, Synopsis, Dissertation, Thesis its Differentiation, References/Bibliography, Technical paper writing/Journal report writing, making presentation, Use of visual aids, Intellectual property, Plagiarism. Research Proposal Preparation: Writing a Research Proposal and Research Report, Writing Research Grant Proposal.

**Suggested Readings:**


1. C.R Kothari, Research Methodology, Methods & Technique, New Age International Publishers, 2004.
2. R. Ganesan, Research Methodology for Engineers, MJP Publishers, 2011.
3. Ratan Khananabis and Suvasis Saha, Research Methodology, Universities Press, Hyderabad, 2015.
4. Y. P. Agarwal, Statistical Methods: Concepts, Application and Computation, Sterling Publs., Pvt., Ltd., New Delhi, 2004.

5. Vijay Upagade and Aravind Shende, Research Methodology, S. Chand & Company Ltd., New Delhi, 2009.
6. G. Nageswara Rao, Research Methodology and Quantitative methods, BS Publications, Hyderabad, 2012.
7. Naval Bajjai, Business Research Methods, Pearson 2011.
8. Prahalad Mishra, Business Research Methods, Oxford 2016.

## 2ECMVL1-13: SIMULATION LAB - II

Draw the Layout, do circuit partitioning, placement and routing, circuit compaction, check DRC, Circuit extraction and finally post layout simulation for different combinational and sequential circuits.

Use the feature of automation test program generation, multilevel logic synthesis for design smaller application chips like multi bit parallel adder priority encoder, general purpose register, ALU, microcontroller/ dsp processor/ traffic light controller /sequential adder etc.

## 2ECMVL4-14: FIELD WORK

Student is required to work in the organization/industry concerned with his/her course.