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7E7081

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7E7081

B.Tech. VII- Semester (Main&Back) Examination, Nov. - 2019
Electronics And Comm. Engg.
7EC1A Antenna And Wave Propagation

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All Questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly.*

UNIT - I

1. a) Describe ideal dipole and short dipole antenna. **(6)**
   b) Describe the difference between directivity and gain. Are they the same in any case? **(4)**
   c) Prove that the radiated power of quarter wave monopole is $P_T = 36.5\, I_{eff}^2$. **(6)**

(OR)

1. a) Draw the equivalent circuit of antenna. Also define the polarisation, antenna front to back ratio (FBR), Antenna band width. **(8)**
   b) Determine the maximum effective aperture and directivity of a short dipole supposed to be operated at f = 450 MHz. **(8)**

UNIT - II

2. a) What are the advantages of array antenna? Describing principle of pattern multiplication and sketch the radiation pattern of a three - element array separated at $\lambda/2$. **(8)**
   b) Calculate the directivity a broad side stacked antenna of height 10.5 m and length 21 m in dB, if operating frequency f = 3.5 GHz. **(8)**

(OR)

2. a) Distinguish between endfire and broadside arrays. Show that array of two isotropic sources fed with equal amplitudes and opposite phases acts as an end - fire array. **(8)**
   b) Describe and draw the radiation pattern of 4-isotropic sources of equal amplitudes and phases in broadside and end-fire arrays. **(8)**

UNIT - III

3. a) Compare half - wave dipole, folded dipole antenna and V - dipole antennas in terms of designs and radiation characteristics. **(8)**

   b) What are the characteristics features of circular end square loop antennas? Write the expressions for their far fields. **(8)**

(OR)

3. a) Describe the principle of operation of Yagi - Uda antenna. Explain its properties with reference to directivity and bandwidth. **(8)**

   b) Describe the design procedure of rectangular patch antenna with a suitable example. Write its applications. **(8)**

UNIT - IV

4. a) Describe the effect of frequency, earth constant and earth curvature on surface wave propagation. **(8)**

   b) Describe the troposphere and troposphere wave propagation. Also justify the statement "Microwave communication is only due to tropospheric propagation". **(8)**

(OR)

4. a) Define the terms surface and elevated ducts and duct gradient. Also describe duct propagation. **(8)**

   b) Show that for space wave propagation the filed intensity at the receiver is given by $E_R = \frac{88\sqrt{P}h_t hr}{\lambda d^2}$ v/m. **(8)**

UNIT - V

5. a) Describe the ionosphere reflection of radio waves. Derive an expression for critical frequency of a reflecting layer in terms of its ionization density. **(8)**

   b) Describe D,E,F, and G layers of the ionosphere. **(4)**

   c) Estimate the maximum electron density of an ionosphere layer for a critical frequency 5.5 GHz. **(4)**

(OR)

5. a) Write notes on virtual height, skip distance, maximum usable frequency, and optimum working frequency. **(8)**

   b) For a mobile communication over a height of 120 km via ionosphere layer with Nmax = 2.22×10^5 electrons/m^3, the maximum frequency estimated to be is 6.5 KHz. Find the optimum working frequency, critical frequency, and elevation angle of beam and path range. **(8)**

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7E7072

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7E7072

B.Tech. VII- Semester (Main & Back) Examination,November - 2019
Electronic Instrumentation & Control Engg.
7EI2A Digital Signal Processing
(Common for AI, EC, EIC)

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 24

Instructions to Candidates:

*Attempt any **five** questions, selecting **one** question from **each unit**. All Questions carry **equal** marks. (sSchematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly) Units of quantities used/calculated must be stated clearly.*

UNIT - I

1. Explain the following using suitable mathematical derivation and wave form

a) Decimation

b) Interpolation **(8+8)**

(OR)

1. a) Obtain the two fold expanded signal y(n) of the input signal x(n)

$$x(n)=\begin{cases}x, x>0\\0, otherwise\end{cases}$$ **(8)**

b) Explain discrete time processing of continuous time signals. **(8)**

UNIT - II

2. Explain the following linear systems

a) Minimum phase system

b) All - pass system. **(8+8)**

(OR)

2. a) Determine H(z) and its poles and zeros if

$$y(n)+\frac{3}{4}y(n-1)+\frac{1}{8}y(n-2)=x(n)+x(n-1)$$ **(8)**

b) Determine the magnitude response of the system given by

$$y(n)+\frac{1}{2}y(n-1)=x(n)-x(n-1)$$ **(8)**

UNIT - III

3. a) Determine direct form I and II for the second order filter given by

$$y(n) = 2b\cos w_0 y(n-1) - b^2 y(n-2) + x(n) - b\cos w_0 x(n-1)$$ **(10)**

b) Explain basic Realisation block diagram and signal flow graph of digital linear system. **(6)**

(OR)

3. Obtain the cascade and parallel realisations for the system function given by

$$H(z) = \frac{1+\frac{1}{4}z^{-1}}{\left(1+\frac{1}{2}z^{-1}\right)\left(1+\frac{1}{2}z^{-1}+\frac{1}{4}z^{-2}\right)}$$ **(16)**

UNIT - IV

4. a) For the analog, transfer function.

$H(s) = \frac{1}{(S+1)(S+2)}$ determine H(z) using impulse invariant technique Assume T = 1S. **(8)**

b) Apply bilinear transformation to $H(s) = \frac{2}{(S+1)(S+3)}$ with T = 0.1 S. **(8)**

(OR)

4. Design a digital Butterworth filter that satisifies the following constraint using bilinear transformation. Assume T = 1S.

$0.9 \le \left|H(e^{jw})\right| \le 1 \quad 0 \le w \le \pi/2$

$\left|H(e^{jw})\right| 1 \le 0.2 \quad \frac{3\pi}{4} \le w \le \pi$ **(16)**

UNIT - V

5. Explain the following :

a) Properties of the DFT

b) DIT Algorithm. **(8+8)**

(OR)

5. Given x(n) = {1,2,3,4,4,3,2,1}

Find x(K) using DIF. FFT Algorithm. **(16)**

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7E7078

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7E7078

B.Tech VII - Semester (Main & Back) Examination, Nov. - 2019
Electronics & Comm. Engg.
7EC3A Digital Image Processing
Common for EC, EIC

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five** questions, selecting **one** question from **each unit**. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used / calculated must be stated clearly.*

UNIT - I

1. a) For a 24-bit color image of size 5 inches by 6 inches, scanning is done at the rate of 300 dots per inches. Calculate the total number of bits required to represent the image. How much time is required to transmit the image if the available data rate is 100 kbps.? **[8]**

   b) Discuss down sampling (or subsampling) and upsampling of an image with suitable example. **[8]**

(OR)

   a) Consider Me image $F = \begin{bmatrix} 1 & 2 \\ 3 & 4 \end{bmatrix}$. Apply image rotation by rotation matrix

$$R = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \text{ choose } \theta = 45^{o}$$ **[8]**

   b) Discuss working of image acquisition system by using CCD sensors. **[8]**

UNIT- II

2. a) Apply histogram, equalisation to the following 4×4 image I_1 and show the resultant image I_2

I_1=

1	3	4	5
5	6	6	6
7	7	7	7
5	5	5	5

Assume image as a 3-bit image. **[8]**

b) An image is represented as under

$$\begin{vmatrix} 5 & 9 & 15 \\ 7 & (2) & 17 \\ 31 & 12 & 14 \\ 7 & 12 & 19 \end{vmatrix}$$

Compute the value of the marked pixel after smoothing by 3×3 average filter. [8]

(OR)

a) Discuss image sharpening by using second order derivative example. [8]

b) Discuss image sharpening (infrequency domain) by Gaussian 2D low pass filter. [8]

UNIT - III

3. a) Justify the statement that median filter is used to minimise salt-and-pepper noise by the following image (use 3×3 median filter)

$$\begin{bmatrix} 24 & 22 & 33 & 25 & 32 & 24 \\ 34 & (255) & 124 & (0) & 64 & 78 \\ 47 & 101 & 10 & 77 & 19 & 69 \end{bmatrix}$$ [10]

b) Write the expression of 2D butterworth high pass filter and discuss its working [6]

(OR)

a) Discuss working of order static filter and their suitable application in image processing. [8]

b) A degradation function is represented as H(u,v). Discuss inverse filtering to improve the image quality after removing bad effects due to degradation function. [8]

UNIT - IV

4. a) Apply image Dilation on the following 5×5 input image by using 3×3 structuring element.

$$\begin{bmatrix} 0 & 1 & 1 & 0 & 1 \\ 1 & 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\begin{bmatrix} 1 & 1 \\ 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix} 0 & 1 & 0 \\ 1 & (1) & 1 \\ 0 & 1 & 0 \end{bmatrix}$$

Input image structuring element [8]

b) Discuss image opening morphological operation by writing its mathematical representation. [8]

(OR)

a) Apply image erosion on the following 5×5 input image by using 3×3 structuring element.

$$\begin{bmatrix} 1 & 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 \end{bmatrix} \qquad \begin{bmatrix} 0 & 1 & 0 \\ 1 & \textcircled{1} & 1 \\ 0 & 1 & 0 \end{bmatrix}$$

Input image structuring element [8]

b) Discuss image closing morphological operation by using its mathematical representation. [8]

UNIT - V

5. a) Discuss watershed transform along with its suitable application. [8]

b) Discuss any one loss less compression technique and state advantages of loss less compression. [8]

(OR)

a) Edge detection mask is defined as

$$\begin{vmatrix} -1 & -1 & -1 \\ -1 & 8 & -1 \\ -1 & -1 & -1 \end{vmatrix}$$

Apply the above mask on the following image

$$\begin{vmatrix} 20 & 49 & 52 & 62 & 70 \\ 55 & 167 & 117 & 161 & 27 \\ 17 & 40 & 51 & 30 & 40 \end{vmatrix}$$ [8]

b) Discuss image segmentation based on global thresholding. [8]

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7E7083

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7E7083

B.Tech. VII- Semester (Main&Back) Examination, Nov. - 2019
Electronics and Communication Engg.
7EC4A Wireless Communication

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five** questions, selecting **one** question from **each unit**. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly.*

UNIT- I

1. a) What is PN sequence? Discuss about the property of PN sequence and also draw a Block diagram to generate 15 length M sequence using flip flop. **(8)**

   b) Explain Transmitter and Receiver of DSSS with suitable diagram. **(8)**

OR

1. a) Explain Fast FHSS and Slow FHSS with an suitable example. **(8)**

   b) The data rate of a DS - CDMA product is f_b = 10Kbps. The spreading rate or chip rate is F_c = 10mbps. How much is jamming margin (Mj) of an output (S/N) of 12 dB is required for a bit error rate (BER) of 10^{-6} performance and given L_{sgs} = 2 dB is system implementation loss. **(8)**

UNIT- II

2. a) Discuss Free space loss shortly. Derive expression for free space loss in dB. **(8)**

   b) Explain Fresnel zone clearance. Find out radius of first Fresnel Zone clearance. **(8)**

OR

2. a) Derive Expression for effective earth radius. **(8)**

   b) Explain all multipath fading channels with their profile in details. **(8)**

UNIT - III

3. a) What are the principle of simplex, Half duplex and full duplex channels explain with Suitable example and diagram. **(8)**

b) Differentiate TDMA, FDMA and CDMA with example. **(8)**

OR

3. a) What do you mean by PRMA? Discuss Aloha protocol with diagram. **(8)**

b) Explain Rake receiver principle and working of the receiver. **(8)**

UNIT - IV

4. a) Explain GSM Network Architecture with working principle. **(8)**

b) Explain need of Mobile IP? How packet delivery perform in mobile IP routing networks explain with diagram. **(8)**

OR

4. a) Explain Bluetooth protocol structure with application. **(8)**

b) Write short note on WLAN and WLL. **(8)**

UNIT - V

5. Explain All parts of Satellite earth station with block diagram and example. **(16)**

OR

5. Write short note on the followings :

i. Keplers law of orbital motion.

ii. LEO, MEO, GEO

iii. Reliability of satellite

iv. Telemetry Tracking and control. **(4×4=16)**

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7E7084

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7E7084

B.Tech. VII- Semester (Main&Back) Examination,November - 2019
Electronics and Comm. Engg.
7EC5A VLSI Design

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All Questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly) Units of quantities used/calculated must be stated clearly.*

UNIT - I

1. a) Develop the relation between I_{ds} and V_{dS} for MOSFET and modify it under channel length modulation. **(8)**

   b) Draw variation of gate oxide capacitance with V_{ds}. Assume the gate voltage $V_{gs} > v_{th}$. **(6)**

   c) State the condition of ohmic operation. **(2)**

OR

1. a) Find the expression of threshold voltage V_{tho} and discuss how it modified under body bias. **(8)**

   b) Discuss any two phenomena in MOSFET from.

   i) Hot electron effect

   ii) Subthreshold conduction

   iii) Narrow channel effect. **(4+4=8)**

UNIT - II

2. a) Draw NMOS inverter with active load and draw its Transfer characteristic. Also find the expression 7 V_{1L}, V_{1H}, V_{OL} and V_{OH} for it. **(10)**

   b) Draw $y = A + \overline{B}C$ using CMOS. **(6)**

OR

2. a) Draw and explain the working of Transmission gate (TG). Use it for 2×1 CMOS multiplexer. **(8)**

b) What is transistor sizing? Design a y = ABC CMOS logic such that its equivalent (D/L) of pull up section is 90 and pull down section is 30. **(8)**

Unit - III

3. a) Draw following CMOS Ckt

   i. y = A+BC+D

   ii. $y = \overline{A} + \overline{BC}$ **(4+4=8)**

   b) Draw the layout of y = AB+CDE CMOS ckt use Eular path in it. **(8)**

OR

3. a) What is Latch up Problem? How it can be avoided in CMOS ckts? **(8)**

   b) State any four DRC rules regarding:

   i. Contact size

   ii. Metal to Metal line separation.

   iii. Poly width and

   iv. Separation between pdiff and Ndiff. **(4×2=8)**

Unit - IV

4. Draw and explain any **two** logic Ckt from.

   i. NORA logic.

   ii. DRAM

   iii. DOMINO logic

   iv. NP logic. **(2×8=16)**

Unit - V

5. Write short note on any **two** :

   i. VHDL code

   ii. FPGA

   iii. Custom design

   iv. ASIC design **(2×8=16)**

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7E7085

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7E7085

B.Tech. VII- Semester (Main and Back) Examination, November - 2019
Electronics and Comm. Engg.
7EC6.1A Advanced Microprocessors
(Common For EC,EIC)

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All Questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly.*

Unit - I

1. a) How many operating modes does 8086 have? Discuss them in brief. **(8)**

   b) With the help of diagram. explain various functional units that 8086 microprocessor contains. **(8)**

OR

1. a) Discuss the register organization of 8086. Explain the function of each register. **(8)**

   b) How many status flags does 8086 have? Discuss the role of each flag. **(8)**

Unit - II

2. a) Explain various software and hardware interrupts supported by 8086 microprocessor. **(8)**

   b) Write an 8086 assembly language program to find the smallest number in an 8 - bit data array. **(8)**

OR

2. a) What are the various addressing modes of 8086 microprocessor. Explain them with suitable example. **(8)**

   b) What are assembler directives? Explain. **(8)**

Unit - III

3. Draw and explain interfacing of ADC 0808/0809 with 8086. Using suitable example. **(16)**

OR

3. a) Draw the block diagram of 8279 keyboard and display controller. Explain its various programming mode. **(8)**

   b) Write short notes on (any two)

   i. 8086 based process control system.

   ii. RS 232 communication standard

   iii. IEEE 488 communication standard **(8)**

Unit - IV

4. a) Draw the internal block diagram of 8255. PPI. Explain the different modes of operation of 8255. **(8)**

   b) Design on interface between 8086 CPU and eight 8 k chips of RAM and four 8 k chips of EPROM. Interface the RAM bank at a segment address OBOOH and the EPRQM bank at a physical address F8000H. **(8)**

OR

4. a) Bring out the difference between static and dynamic RAM. Describe the procedure of interfacing static memories with a CPU. **(8)**

   b) Draw and explain the architecture of 8257 DMA controller. **(8)**

Unit - V

5. a) What is the difference between multi tasking and multiuser operating system Explain in brief. **(8)**

   b) Discuss the software design aspects of multimicroprocessor system. **(8)**

OR

5. Write short note on any **two** :

   i. 80286 processor

   ii. 80386 processor

   iii. 80486 processor

   iv. Pentium processor **(2×8=16)**

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7E7077

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7E7077

B.Tech. VII - Semester (Main&Back) Examination, Nov. - 2019
Electronics & Comm. Engg.
7EC6.2A Artificial Intelligence and Expert Systems
(Common For EC,EIC)

Time : 3 Hours **Maximum Marks : 80**
Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five** questions, selecting **one** question from **each unit**. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly.*

UNIT - I

1. a) Briefly give Introduction of artificial Intelligence. **(8)**
   b) Explain uninformed search and informed search in brief. **(8)**

(OR)

1. a) Explain constraint satisfaction problems in Artificial intelligency. **(8)**
   b) Explain the engineering goal of AI. **(8)**

UNIT - II

2. a) Define concept of knowledge and also explain the Representation of Knowledge. **(8)**
   b) Briefly explain first order logic for knowledge representation. **(8)**

(OR)

2. Write short note on - **(2×8=16)**
   a) Inference in propositional logic.
   b) Resolution in FOPL.

Unit - III

3. a) Explain the various components of a planning system. **(8)**
   b) Write short note on Forward Versus backward Reasoning. **(8)**

OR

3. Explain the following in terms of knowledge organization - (2×8=16)

a) Rule Based system.

b) Reasoning in semantic Net frames.

Unit - IV

4. a) What are the components of an expert system? Explain in brief. (8)

b) Explain the characteristics of a good expert system. (8)

OR

4. a) Define and Explain rule based expert system. (8)

b) What are the implementation issues with Reasoning under uncertainty. (8)

Unit - V

5. a) Explain the single layer and multi - layer neural network with suitable example.(8)

b) What do you mean by learning process? Explain reinforcement learning. (8)

OR

5. Write short note on (any **two**) : (2×8=16)

a) Natural language processing.

b) Probabilistic learning

c) Rule Induction and Decision trees.

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7E7086

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7E7086

B.Tech. VII -Semester (Main&Back) Examination, Nov. - 2019
Electronics And Comm. Engg.
7EC6.3A VHDL

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 26

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All Questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly). Units of quantities used/calculated must be stated clearly.*

UNIT - I

1. a) What is the difference between CPLD and FPGA? Explain both of them according to their applications. **(10)**

   b) What is routing? Explain briefly. **(6)**

(OR)

1. a) Write about the design flow for ASIC. **(8)**

   b) State the difference between synthesis and simulation and explain the logic synthesis in detail. **(8)**

UNIT - II

2. Define the following in VHDL :

   i) Entity

   ii) Architecture

   iii) Package

   iv) Configuration **(16)**

(OR)

2. a) What is VHDL? Explain advantage and limitations of VHDL. **(8)**

   b) Write short note on

      i. Behavioral Modelling

      ii. Structural modelling. **(8)**

UNIT - III

3. a) Write a VHDL code for 1:16 line decoder. (8)

b) Consider the function

$$Y = \bar{A}BC + \overline{ABC} + AB\bar{C}$$

Impliment the above function using 2:1 multiplexer and also write the VHDL code for it. (8)

(OR)

3. Write a VHDL code for following :

á. JK flip flop

b. D flip flop using JK flip flop.

c. T flip flop

d. 3 - Input XOR gate. (16)

UNIT - IV

4. a) What is finite state machine : (4)

b) Design a moore type FSM to detect 101 non overllaping sequence. Also design the synchronous sequential circuit using D - flip flop. (12)

(OR)

4. a) Write a VHDL code for serial adder. (8)

b) State the difference between mealey and moore type FSM. (8)

UNIT - V

5. a) Draw a schematic diagram of data path circuit for multiplier operation. (8)

b) What problems occur during clock synchronization? Also explain the techniques to avoid them. (8)

(OR)

5. a) What is memory organization? Explain 6 T SRAM in detail. (8)

b) How external devices are interfaced with CPU? Explain in detail. (8)